High Density European RH SRAM-based FPGA
1st validated prototypes - BRAVE

Prime: NanoXplore (FR), SubContractor(s): STMicroelectronics(FR)
Alpha customers: AirbusDS (DE, FR, ES, GB), TAS (FR, IT, ES, GB)

<table>
<thead>
<tr>
<th>TRP</th>
<th>TRP 4000113670/15/NL/LvH</th>
<th>YoC: 2017</th>
<th>TRL</th>
<th>Initial: X</th>
<th>Current: X</th>
<th>Target TRL: X Date: Q1 2017</th>
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<tr>
<td>ESA Budget</td>
<td>Co-funded Budget:</td>
<td>1,600 k€</td>
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<td></td>
<td></td>
<td>1,700 k€</td>
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</table>

TO: David Merodio Codinachs (TEC-EDM)

Background and justification:
Field Programmable Gate Arrays (FPGAs) are versatile components that implement a wide range of digital functions and are present in almost all digital electronic units across all ESA missions. The need for competitive European FPGAs that enable flexibility, high performance and miniaturization has been harmonized with agencies and the space industry. This strategic development has been originally defined and co-funded between ESA and CNES.

Objective(s):
The goal of this activity is to define, design, verify, manufacture and validate the first medium-capacity, high-performance, radiation-hardened re-programmable European FPGA (NG-MEDIUM) and its development kit.
It is the first FPGA of the Big Re-programmable Array for Versatile Environments (BRAVE) FPGA family.

Achievements and status:
The BRAVE NG-MEDIUM has been designed, verified, manufactured using 65nm CMOS technology from STMicroelectronics. The NG-MEDIUM prototypes have been functionally validated.
Two radiation test campaigns have confirmed the expected radiation performance that has been achieved using Radiation Hardened By Design (RHBD) techniques.
The Development Kit has been designed, manufactured and integrated; and is available for customers.
The FPGA tools have been developed self-funded by NanoXplore (budget not included in the slide).

Benefits:
This first BRAVE FPGA provides a competitive solution to develop electronic units for space. It is already being analyzed by a large number of companies. The BRAVE FPGAs flexibility through re-programmability, miniaturization and faster performance are key enabler of the Space 4.0.
BRAVE consortium

- NanoXplore and ST partners
  - **NanoXplore**
    - Design, Verify and Bring up (validation);
    - FPGA tools
  - **STm**
    - Foundry,
    - IP provider,
    - Packaging Evaluation & Qualification

- Alpha Customers
  - **Airbus D&S, TAS**
    - Key alpha customers involved since the beginning of the project
NanoXplore rad-hard FPGA offering is supported by its own software NanoXmap

- Fully integrated flow from synthesis down to bit stream generation and reports (timing, LUTs utilization etc)
- NanoXmap is already released and meet the initial expectations
  - Utilization rate >80%
  - Best compilation time of the market

- Support
  - Verilog IEEE 1364-1995/2001 and
  - VHDL IEEE 1076 – 1993 / 2008
**Process Technology: STM C65 SPACE**

**Features**

**Process**
- ST/microelectronics C65SPACE (65nm CMOS)
- 3.3V IO gate oxide GO2 (5nm)
- 1.2V core gate oxide GO1 (1.9nm), triple VT transistors
- 7 copper metallization: 5 thin and 2 thick
- Low-K inter-metallic dielectrics for thin metal layers
- High density SRAMs
- Compatible with flip-chip and wire bonding packaging

**Radiations**
- SEL-free up to LET = 60MeV/μm/cm² at 125°C Tj and Vdd max
- SEE hardened library
- Tested up to a total dose of 300 krad (Si)

**Reliability**
- Library cells models with 20 years aging
- Transistor models including aging alteration
- ESD better than:
  - 2kV in HBM (Class 2 / MIL-STD-883H)
  - 150V in MM
  - 250V in CDM

**Library offer**
- Comprehensive library of standard logic with P/V and aging corners models
- IO pad libraries provide interfaces at 3.3V +/- 0.3V, 2.5V +/- 0.25V and 1.8V +/- 0.15V
- High speed IO Pad LVDS supplied at 2.5V +/- 0.25V up to 500Mbps
- Cold sparing ICs with single/double row support
- Memories generation: single port SRAM, ROM, Dual port SRAMs, BIST library, EDAC library
- Wide-range PLLs 1.2GHz with multi-phase outputs
- 6.25Gbit/s high speed serial links (HSSL)

**Design flow**
- An ST customized design flow (RTL to GDS)
  - Invoking commercial solutions (Synopsys, Cadence, Mentor, ...)
  - Available for partners and certified design houses:
    - Front-End kit from RTL to gates based
    - SiPKit for IO ring generation
    - FTK for place and route
    - SignOffKit for final verification before tape-out
  - For customer owned tools (COT) flow, ST provides the C65SPACE design platform along with the DRM and sign-off kit.

**Description**
The C65SPACE is fabricated on a proprietary 65nm, 7 metal layers CMOS process intended for use with a core voltage of 1.2V ±0.1V.
The ST standard-cells, memories and PLL have been designed and characterized to be compatible with each other.
NX FPGAs are Rad Hardened

All logic of NX FPGAs is hardened by design (RHBD) and simulated with TFIT software

On top of it,
Embedded Configuration Memory Integrity Check ("CMIC")
CMIC Overview

**CMIC= Configuration Memory Integrity (= Scrubber Ctrl)**

- The CMIC is an embedded engine performing automatic verification and repair of the configuration memory.
- A CMIC reference memory is initialized during the bit stream download process with reference data computed by the NanoXmap software.
- Once the initialization is done, the CMIC engine can be periodically activated to perform the following sequence:
  - 1. Read configuration data
  - 2. Calculate signature
  - 3. Compare the signature with CMIC reference
  - 4. If a mismatch is detected:
    - a. Calculate faulty address (BAD @) and faulty bit location
    - b. Read DATA[BAD @]
    - c. Repair flipped bit
    - d. Write DATA[BAD @]
- The CMIC period can be set by the user. The **minimum period is 5.3 ms** and the maximum 65 days. The configuration memory scan takes 4ms.
- The **CMIC reference memory is protected by ECC**.
- The CMIC does not need to access the external NVRAM when performing checks and repairs at run time.
### Device Details

<table>
<thead>
<tr>
<th>Device</th>
<th>Details</th>
<th>NX1H35</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Capacity</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ASIC Gates</td>
<td></td>
<td>550 000</td>
</tr>
<tr>
<td><strong>Modules</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Register</td>
<td>3* Tile + 2*GBs</td>
<td>32 256</td>
</tr>
<tr>
<td>LUT-4</td>
<td>4<em>28</em>3 rows</td>
<td>34 272</td>
</tr>
<tr>
<td>Carry</td>
<td>9<em>28</em>3 rows</td>
<td>8 064</td>
</tr>
<tr>
<td><strong>Embedded RAM (Mb)</strong></td>
<td></td>
<td>2.8Mb</td>
</tr>
<tr>
<td>DPRAM</td>
<td>56*48Kb</td>
<td>2.688K</td>
</tr>
<tr>
<td>Core Register File</td>
<td>28<em>2</em>3 rows</td>
<td>168</td>
</tr>
<tr>
<td>Core Register File Bits</td>
<td>16<em>2</em>(16+6) bits</td>
<td>116K</td>
</tr>
<tr>
<td><strong>Embedded DSP</strong></td>
<td></td>
<td>112</td>
</tr>
<tr>
<td><strong>Embedded Serial Link</strong></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>SpaceWire link 400Mbps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SERDES</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td><strong>Hard IP Processor</strong></td>
<td></td>
<td>NO</td>
</tr>
<tr>
<td><strong>I/O PHY</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR</td>
<td></td>
<td>16</td>
</tr>
<tr>
<td>SpaceWire</td>
<td></td>
<td>16</td>
</tr>
<tr>
<td><strong>I/Os</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O banks</td>
<td>8 Complex + 5 Simple</td>
<td>13</td>
</tr>
<tr>
<td>User I/Os</td>
<td></td>
<td>380</td>
</tr>
<tr>
<td>LGA-625 / CGA-625</td>
<td></td>
<td>180</td>
</tr>
<tr>
<td>CQFP-352</td>
<td></td>
<td>TBD</td>
</tr>
<tr>
<td>CQFP-256</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
First rad-hard FPGA developed in STM 65nm bulk

Performance:
- Logic: 200MHz
- DSP: 333MHz
- I/O: 800Mbps

Class-1 to Class-3 qualification
- LGA-625
- CQFP-352

Hardening performance (RHBD)
- Fully hardened by design
- Total dose > 300 Krads TID
- No SEL for LETth>60 MeV-cm² / mg)
- SER / device.day 1,70e-4
Bring up
- Samples received August 2016
- Functional tests mostly finalized
- One metal fix M1 required to fix a bug on the I/Os

Packaging
- LGA 625 available, ‘Prototype level’
- CQFP 352 developed for QML qualification expected Nov2017,

Hardening
- First radiative test done in October 2016:
  ➔ memory configuration test done – SER / day device level 1.70e-4
- Second radiative test campaign done end of November 2016:
  ➔ DFF static and dynamic test, CMIC and DPRAM

NanoXmap
- Synthesis, mapping and place & route tools flow – available
- Timing driven flow – available 2017
- Optimization phase, incl. DSP advanced tools – Q4 2017
**LGA625**
29*29mm body, 1,00mm pitch

**MQFP352**
48*48mm body, 0,50mm pitch

MQFP256 in the pipe
The DevKit is an evaluation board to be used interactively through JTAG, or standalone from a EEPROM board.

The board configuration mode is thus selected by on-board jumpers.

A 10-pin HE10 connector is provided to receive an EEPROM memory board (Atmel Dump Mode EEPROM or standard SPI EEPROM).

An optional SpaceWire connector allows SpaceWire configuration.
Bitstream Interfaces

- JTAG
- Slave SpaceWire
- Slave // 8 bits
- Slave // 16 bits
- Master SPI
- Master Dump

Bitstream Download
SEE campaign

- 2 SEE campaigns done in Q4CY16
  - 1st silicon used, out of wfab in Summer-16,
  - Packaged in LGA625 tested,
  - First radiative test done in October 2016:
    ➞ memory configuration test done – SER / day device level 1.70E-4
  - Second radiative test campaign done end of November 2016:
    ➞ DFF static and dynamic test, CMIC and DPRAM
## SEE campaign

### Ion Beam (High penetration ions):

<table>
<thead>
<tr>
<th>Ion</th>
<th>DUT energy [MeV]</th>
<th>Range [μm Si]</th>
<th>LET [MeV/mg/cm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$^{13}$C$^{4+}$</td>
<td>131</td>
<td>269.3</td>
<td>1.3</td>
</tr>
<tr>
<td>$^{14}$N$^{4+}$</td>
<td>122</td>
<td>170.8</td>
<td>1.9</td>
</tr>
<tr>
<td>$^{22}$Ne$^{7+}$</td>
<td>238</td>
<td>202.0</td>
<td>3.3</td>
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<tr>
<td>$^{27}$Al$^{8+}$</td>
<td>250</td>
<td>131.2</td>
<td>5.7</td>
</tr>
<tr>
<td>$^{40}$Ar$^{12+}$</td>
<td>379</td>
<td>120.5</td>
<td>10.0</td>
</tr>
<tr>
<td>$^{53}$Ni$^{18+}$</td>
<td>513</td>
<td>107.6</td>
<td>16.0</td>
</tr>
<tr>
<td>$^{58}$Ni$^{18+}$</td>
<td>582</td>
<td>100.5</td>
<td>20.4</td>
</tr>
<tr>
<td>$^{84}$Kr$^{25+}$</td>
<td>769</td>
<td>94.2</td>
<td>32.4</td>
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<tr>
<td>$^{124}$Ni$^{35+}$</td>
<td>995</td>
<td>73.1</td>
<td>62.5</td>
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</table>

Radiations: SEU / SET Tests Overview

- Temperature measured 19-\(\rightarrow\)34° C
- Supply at their min value (-10\%):
  - VDD1V2 Core supply 1.08V
    - No voltage sensor-\(\rightarrow\)1.045V inside the chip.
- Angular cross-section for config given in chip plan
- Normal incidence for other tests
- Fluence over \(10^6\) p/cm\(^2\) for config, static DFF, dynamic DFF

<table>
<thead>
<tr>
<th>Test</th>
<th>Devices under test</th>
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<tr>
<td>Config SEU</td>
<td>6 138 096 configuration memory</td>
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<tr>
<td>DPRAM SEU</td>
<td>56 DPRAM with EDAC ST_DPHD_2048x24m4_b = 2 752 512 bit</td>
</tr>
<tr>
<td>DFF static</td>
<td>32 256 DFF</td>
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<tr>
<td></td>
<td>1008 matrix system output of the clock tree</td>
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</table>
Radiations: SEU / SET Tests Results

- Chess-board pattern
- SER normal incidence
- LET: 10 -> 62.5 Mev.cm²/mg

- CREAME 96 model for SER calculation:
  - GEO
  - solar min
  - shielding = 100mils
  - sensitive volume thickness = 2µm
  - Unhardened SRAM SER /9400

<table>
<thead>
<tr>
<th>Weibull parameter chip6+7</th>
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<tr>
<td>SIGsat (cm²/bit)</td>
<td>5.1852E-09</td>
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<tr>
<td>L0 (MeV/(mg/cm²))</td>
<td>0.11214</td>
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<tr>
<td>W (MeV)</td>
<td>36.4286</td>
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<tr>
<td>s</td>
<td>4.44737</td>
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<table>
<thead>
<tr>
<th>Configuration Memory SEU @ 30°C,1.045V</th>
<th>SER</th>
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<tbody>
<tr>
<td>SEU/config/day</td>
<td>2.7E-11 SEU/config/day</td>
</tr>
<tr>
<td>SEU/chip/day</td>
<td>1.7E-04 SEU/chip/day</td>
</tr>
<tr>
<td>SEU/chip/year</td>
<td>6.1E-02 SEU/chip/year → SER 16years</td>
</tr>
</tbody>
</table>
Radiations: Config SEU

**SEU config cross-section (LET) of chip 6 & 7**

![Graph showing SEU config cross-section (LET) of chip 6 & 7.](image)
Radiations: Static DFF SEU, clock SET

- 4 combination input output for DFF -> interleaved pattern
- Clock SET cross-section overestimation -> SET = SET propagating at one output (mtx_sys) of the clock tree to the 32 driven DFF

![Graph showing dff SEU clock SET cross-section (LET)](image-url)

**Graph Details:**
- SEU config BRAVE#6
- SET Xs 2 decade under config XS
- DFF SEU Xs 3 decade under config XS
Radiations: EDAC Results

- Double error cross section two decades lower than these of config
- 6 138 096 config > 2 752 512 DPRAM bit

→ Chip level: DPRAM SER << config SER

**SEU cross-section DPHD**

![Graph showing SEU cross-section vs LET Eff (MeV/(mg/cm²))](image)

- **SEU ST_DPHD_2048x24m4_b**
- **Uncorrected double error ST_DPHD_2048x24m4_b**
Radiations: CMIC Results

- No double error recorded in the EDAC reference memory ST_SPREG_144x27m4

![Diagram showing SEU config cross-section (LET) with CMIC]

- SEU config BRAVE#6 with CMIC
- SEU config BRAVE#6 without CMIC
- SEU config double error in same signature BRAVE#6

>1 decade
High Density European RH SRAM-based FPGA Achievements & Status

- NanoXmap is available **NOW** free-of-charge against a Software Licence Agreement (SLA) approved and signed,
- NG-Medium prototypes packaged in LGA625 (NX1H35S-LG625PR) are available ‘**NOW**’,
- NG-Medium evaluation kit (NX1H35-EK) is available ‘**NOW**’.

**NG** medium can be selected for Spaceborne applications **NOW**, as soon as the relevant project can assume EM & FM parts becoming available respectively Dec17 and Sep18 best case (*).

(*) Manufacturing in parallel with Space Qualification parts
High Density European RH SRAM-based FPGA
Next Step 1 – NanoXmap evaluation
## High Density European RH SRAM-based FPGA

Next Step 2 – BRAVE Qualification

<table>
<thead>
<tr>
<th>Description</th>
<th>P/N</th>
<th>When</th>
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<tr>
<td>Design Suite</td>
<td>NanoXmap</td>
<td>NOW</td>
</tr>
<tr>
<td>Datasheet</td>
<td>NX1H35_ds-v1.1.pdf</td>
<td>NOW</td>
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<tr>
<td>Evaluation Kit</td>
<td>NX1H35-EK</td>
<td>Mar-17</td>
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<tr>
<td>Prototype</td>
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<tr>
<td></td>
<td>NX1H35S-LG625PR</td>
<td>NOW</td>
</tr>
<tr>
<td></td>
<td>NX1H35S-CQ352PR</td>
<td>Nov17</td>
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<tr>
<td></td>
<td>NX1H35S-CQ256PR</td>
<td>Q1CY17</td>
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<td>EM part (Mil. Temp)</td>
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<td>NX1H35S-LG625M</td>
<td>Q1CY18</td>
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<td>NX1H35S-CQ352M</td>
<td>Dec17</td>
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<tr>
<td></td>
<td>NX1H35S-CQ256M</td>
<td>Q1CY18</td>
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<tr>
<td>EQM part (eq. QML-Q)</td>
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</tr>
<tr>
<td></td>
<td>NX1H35S-LG625Q</td>
<td>Q3CY18</td>
</tr>
<tr>
<td></td>
<td>NX1H35S-CQ352Q</td>
<td>Q3CY18</td>
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<tr>
<td></td>
<td>NX1H35S-CQ256Q</td>
<td>Q3CY18</td>
</tr>
<tr>
<td>FM part (eq. QML-V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>NX1H35S-LG625V</td>
<td>Q3CY18</td>
</tr>
<tr>
<td></td>
<td>NX1H35S-CQ352V</td>
<td>Q3CY18</td>
</tr>
<tr>
<td></td>
<td>NX1H35S-CQ256V</td>
<td>Q3CY18</td>
</tr>
</tbody>
</table>

Red Color= Base line QML-V qualification
High Density European RH SRAM-based FPGA
Next Step 3 – Pursue FPGA development

FPGA Performance (MHz)

Higher Performances
Lower Power Consumption
Lower SER

kLUT4 density

65nm
NG-MEDIUM
NX1H35
(EU)

65nm
NG-LARGE
NX1H40
(EU)

RTG4 (US)
65nm

V4QV (US)
90nm

V5QV (US)

150nm
RTAX200m
(US)

150nm
E3000L
(US)

Next step
NG-ULTRA

#25
ESA Space Engineering & Technology Final Presentation Days – Noordwijk, NL – 24may17
Conclusion

Questions & Answers
Thank you